DATAFLOW GRAPH COMPRESSION FOR POWER REDUCTION IN A VECTOR PROCESSOR

ABSTRACT OF THE DISCLOSURE

A method and apparatus for power reduction in a processor controlled by multiple-instruction control words. A multiple-instruction control word comprises a number of ordered fields, with each ordered field containing an instruction for an element of the processor. The sequence of instructions for a loop is compressed by identifying a set of aligned fields that contain NOP instructions in all of the control words of the sequence. The sequence of control words is then modified by removing the fields of the identified aligned set containing NOP instructions and adding an identifier that identifies the set of fields removed. The sequence of control words is processed by fetching the identifier at the start the loop, then, for each control word in the sequence, fetching a control word and reconstructing the corresponding uncompressed control word by inserting NOP instructions into the compressed control word as indicated by the identifier. The identifier may be a bit mask and may used to disable memory units and processing elements for the duration of the loop to reduce power consumption by the processor.